1. (Fourth Amendment) An apparatus comprising:

a transistor having an enable terminal, an input terminal, and an output terminal, said input terminal coupled to receive binary signals that vary between first and second preselected voltage levels, and said output terminal coupled to deliver binary signals that vary between the first preselected voltage level and a third preselected voltage level;

a capacitor coupled across said input and output terminals of said transistor; and

a resistive element having a first end portion coupled to the enable terminal of said transistor and a second end portion coupled to a voltage supply to bias the transistor continuously on, the resistive element cooperating with a parasitic capacitor defined by said transistor to increase the voltage applied to the enable terminal during a transition from the first to the second preselected voltage level at the input terminal.

8. (Third Amendment) An apparatus for converting first digital signals that vary between [0 volts and a first preselected voltage level] a first and second preselected voltage levels to second digital signals that vary between [0 volts and a second] the first and a third preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain [for receiving] coupled to receive said first signals [that vary between 0 volts and the first preselected voltage level], said source [for delivering] coupled to deliver said second signals [that vary between 0 volts and the second preselected voltage level], said gate coupled to a voltage supply [having a third preselected voltage level];

a capacitor coupled across said source and drain of said pass gate transistor; and

a pump coupled to the gate of said pass gate transistor, said pump being configured to increase the voltage level applied to said gate during a transition from [0 volts to the first preselected voltage level] the first to the second preselected voltage levels.

9. (Third Amendment) An apparatus, as set forth in claim 8, wherein said pump includes a resistive element coupled between the gate of said pass gate transistor and said voltage supply, and a capacitor coupled to the gate of said pass gate transistor to receive said first digital signals [that vary between 0 volts and the first preselected voltage level].

13. (Third Amendment) An apparatus for converting an input signal that varies between first and second preselected voltage levels to an output signal that varies between the first preselected voltage level and a third preselected voltage level, comprising:

a pass gate transistor having a gate, source, and drain, said drain [for receiving] coupled to receive said input signal[s], said source [for delivering] coupled to deliver said output signal[s], said gate being coupled to a voltage supply [having a fourth preselected voltage level];

a capacitor coupled across said source and drain of said pass gate transistor; and

means for increasing the voltage level applied to said gate during a transition of the input signal from the first to the second preselected voltage level.

17. (First Amendment) A buffer circuit, comprising:

a pass gate transistor having a gate, source, and drain, said drain coupled to receive a first digital signal that varies between first and second voltage levels;

a first voltage supply coupled to the gate of said pass gate transistor to bias the transistor continuously on;

a capacitor coupled across the source and drain of said pass gate transistor;

an inverter having an input terminal and an output terminal, said input terminal coupled to the source of said pass gate transistor to receive a second digital signal that varies between the first voltage level and a third voltage level; [and]

a pull-up transistor having a source coupled to a second voltage supply, a drain coupled to the source of said pass gate transistor, and a gate coupled to the output terminal of said inverter[.]; and

a resistive element coupled between said first voltage supply and the gate of said pass gate transistor, the resistive element cooperating with a parasitic capacitor defined by the drain and gate of said pass gate transistor to increase the applied voltage to the gate of said pass gate transistor.

In claim 19, line 1, replace "18" with –17--.

In claim 20, line 1, replace "18" with –17--.